International Journal of Electrical and Electronics Engineering Research (IJEEER)
ISSN(P): 2250-155X; ISSN(E): 2278-943X
Vol. 4, Issue 2, Apr 2014, 107-112
© TJPRC Pvt. Ltd.

TRANS STELLAR
• Journal Publications • Research Consultancy

MODELLING OF CMOS MEMORY CELL TO REDUCE SOFT ERRORS

R.PRIYADHARSINI

Sri Eshwar College of Engineering, Coimbatore, Tamil Nadu, India

ABSTRACT

The tremendous scaling of CMOS technology necessitates reliable operation for many circuit designs. Due to the lower Vdd and the smaller node capacitance, the amount of charge stored on a circuit node is becoming increasingly smaller, thus making circuits more susceptible to spurious voltage variations caused by externally induced phenomena such as cosmic ray neutrons. This project proposes a new hardening design for an 11 transistors (11T) CMOS memory cell at 32 nm feature size. The proposed hardened memory cell overcomes the problems associated with the previous design by utilizing novel access and refreshing mechanisms. Simulation shows that the data stored in the proposed hardened memory cell does not change even for a transient pulse of more than twice the charge than a conventional memory cell. Moreover it achieves 55% reduction in power delay product compared to the DICE cell (with 12 transistors) providing a significant improvement in soft error tolerance. Simulation results are provided using the predictive technology file for 32 nm feature size in CMOS.

KEYWORDS: Tremendous Scaling of CMOS Technology, DICE Cell, Single-Event Transient (SET)